85. (new) The data storage system of claim 84 wherein the regular memory cells are configurable to store one of 2^N values, where N is 2 or greater and the spare memory cells are configurable to store one of 2^N values.

86. (new) The data storage system of claim 84 wherein the regular memory cells are configurable to store one of 2^N values, where N is 2 or greater, and the spare memory cells are configurable to store one of two values.

87. (new) The data storage system of claim 84 wherein the spare memory array stores overhead data.

88. (new) A data storage system comprising:

a plurality of regular memory arrays, each regular memory array including a plurality of memory cells;

a plurality of regular y-drivers, each regular y-driver being coupled to a corresponding one of the plurality of regular memory arrays, each regular y-driver configured to control bitlines of said memory array;

a spare memory array including a plurality of spare memory cells; and

a spare y-driver coupled to the spare memory array configured to control said bitline of the spare memory array.

89. (new) The data storage system of claim 88 wherein the regular memory cells are configurable to store one of 2^N values, where N is 2 or greater and the spare memory cells are configurable to store one of 2^N values.

90. (new) The data storage system of claim 88 wherein the regular memory cells are configurable to store one of 2^N values, where N is 2 or greater, and the spare memory cells are configurable to store one of two values.

91. (new) The data storage system of claim 88 wherein the spare memory array stores overhead data.

92. (new) A data storage comprising:

a plurality of regular memory arrays, each regular memory array including a plurality of regular memory cells;

at least one regular memory decoder coupled to the regular memory arrays, each regular memory decoder configured to provide bias signals to selected ones of the plurality of regular memory cells;

a regular address predecoder coupled to the at least one regular memory decoder to provide selection signals to the at least one regular memory decoder in response to a first address signal;

a spare memory array, each spare memory array including a plurality of spare memory cells;

a spare memory decoder coupled to the spare memory array and configured to provide bias signals to selected ones of the plurality of spare memory cells of said spare memory array; and

a spare address predecoder coupled to the spare memory decoder to provide selection signals to the spare memory decoder in response to a spare address signal.

93. (new) A data storage system comprising:

a plurality of regular memory arrays, each regular memory array including a plurality of regular memory cells, wherein each regular memory cell is configurable to store one of 2^N values, where N is 2 or greater;

a plurality of spare memory arrays, each spare memory array including a plurality of spare memory cells, wherein each spare memory cells is configurable to store one of 2^N values, where N is 2 or greater;

at least one memory decoder coupled to the regular and spare memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of regular and spare memory cells; and

a reference array operatively coupled to the regular and spare memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells, the spare memory array being configurable to provide at least one of said reference signals.

94. (new) A data storage comprising:

a plurality of regular memory arrays, each regular memory array including a plurality of regular memory cells;

a spare memory array, each spare memory array including a plurality of spare memory cells; and

a decoder coupled to the regular memory arrays and the spare memory array and configured to select ones of the plurality of regular and spare memory cells in response to input data bits; and

a controller coupled to the regular memory arrays and the spare memory array to apply first programming signals to said selected ones of the regular memory cells and to apply second programming signals to said selected ones of the spare memory cells.

95. (new) A data storage comprising:

a plurality of regular memory arrays, each regular memory array including a plurality of regular memory cells;

a spare memory array, each spare memory array including a plurality of spare memory cells; and

a decoder coupled to the regular memory arrays and the spare memory array and configured to select ones of the plurality of regular and spare memory cells in response to input data bits; and

a controller coupled to the regular memory arrays and the spare memory array to apply first read signals to said selected ones of the regular memory cells and to apply second read signals to said selected ones of the spare memory cells.

96. (new) A data storage comprising:

a plurality of regular memory arrays, each regular memory array including a plurality of regular memory cells;

a spare memory array, each spare memory array including a plurality of spare memory cells; and

a decoder coupled to the regular memory arrays and the spare memory array and configured to select ones of the plurality of regular and spare memory cells in response to input data bits; and

a controller coupled to the regular memory arrays and the spare memory array to apply first erase signals to said selected ones of the regular memory cells and to apply second erase signals to said selected ones of the spare memory cells.

97. (new) A data storage comprising:

a plurality of regular memory arrays, each regular memory array including a plurality of regular memory cells;

a spare memory array, each spare memory array including a plurality of spare memory cells; and

a decoder coupled to the regular memory arrays and the spare memory array and configured to select ones of the plurality of regular and spare memory cells in response to input data bits; and

a controller coupled to the regular memory arrays and the spare memory array to apply first verify signals to said selected ones of the regular memory cells and to apply second verify signals to said selected ones of the spare memory cells.

98. (new) A data storage system comprising:

a plurality of multidimensional segmented regular memory arrays, each regular memory array including a plurality of regular memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each regular memory cell is configurable to store one of 2^N values, where N is 2 or greater;

a plurality of multidimensional segmented spare memory arrays, each spare memory array including a plurality of spare memory cells, a plurality of bitlines, a plurality of control

gate lines, and at least one common line, wherein each spare memory cells is configurable to store one of 2^N values, where N is 2 or greater;

at least one memory decoder coupled to the regular and spare memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of regular and spare memory cells; and

a reference array operatively coupled to the regular and spare memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the plurality of memory cells.

99. (new) An integrated circuit data storage system comprising:

a plurality of regular memory cells, each regular memory cell being configurable to store one of a plurality of signal levels;

a first decoding circuit coupled to the plurality of regular memory cells and configured to generate first and second control signals based on a first set of input data bits; and

a first supply source operatively coupled to selected ones of the plurality of regular memory cells based on the first control signal from the decoding circuit, the first supply source configured to provide first programming signals based on the second control signal,

a plurality of spare memory cells, each spare memory cell being configurable to store one of a plurality of signal levels;

a second decoding circuit coupled to the plurality of spare memory cells and configured to generate third and fourth control signals based on a second set of input data bits;

a second supply source operatively coupled to selected ones of the plurality of spare memory cells based on the third control signal from the second decoding circuit, the second supply source configured to provide second programming signals based on the fourth control signal,

wherein the selected regular and spare memory cells are programmed in accordance with the programming signals from the first and second supply sources, respectively.

100. (new) A multilevel memory system comprising:

a multilevel integrated circuit memory unit that includes:

a plurality of regular memory cells, each regular memory cell being programmable to one of a plurality of levels in response to a first set of programming signals,

a first decoding circuit coupled to the plurality of regular memory cells and configured to generate first and second control signals based on a first address,

a first supply source coupled to selected ones of the plurality of regular memory cells based on the first control signal, the first supply source configured to provide the first set of programming signals based on the second control signal,

a plurality of spare memory cells, each spare memory cell being programmable to one of a plurality of levels in response to a second set of programming signals,

a second decoding circuit coupled to the plurality of spare memory cells and configured to generate third and fourth control signals based on a second address, and

a second supply source coupled to selected ones of the plurality of spare memory cells based on the third control signal, the second supply configured to provide the second set of programming signals based on the fourth control signal; and

a microcontroller coupled to the memory unit and operative to control operation of the memory unit.

101. (new) A data storage system comprising:

a plurality of segmented regular memory arrays, each regular memory array including a plurality of regular memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each regular memory cell is configurable to store one of 2^N values where N is 2 or greater;

a plurality of segmented spare memory arrays, each spare memory array including a plurality of spare memory cells, a plurality of bitlines, a plurality of control gate lines, at least one common line, wherein each spare memory cell is configurable to store one of 2^M power values, where M is 2 or greater;

at least one memory decoder coupled to the regular and spare memory arrays, each memory decoder configured to provide bias signals to selected ones of the pluralities of regular and spare memory cells; and

a reference array operatively coupled to the regular and spare memory arrays and configurable to provide reference signals used for programming and reading the selected ones of the pluralities of regular and spare memory cells.

102. (new) A method for programming a multilevel regular memory cell and an spare memory cell to a corresponding one of a plurality of levels, the method comprising:

receiving a plurality of data bits;

determining first and second comparison values corresponding to the received data bits;

placing the regular and spare memory cells in a voltage mode;

verifying the regular memory cell using the first comparison value;

after the verifying, if programming is required, programming the regular memory cell with a program value;

verifying the spare memory cell using the second comparison value; and

after the verifying of the spare memory cell, if programming is required, programming the spare memory cell with another program value.

103. (new) The method of claim 102, wherein the verifying includes:

sensing a voltage value stored in the regular memory cell,

comparing the values sensed from the regular memory cell with a first comparison value,

sensing the voltage value stored in the spare memory cell, and

comparing the values sensed from the spare memory cell with the second comparison value,

wherein the sensing includes:

applying a first voltage on a common line coupled to the regular memory cell,

applying a second voltage on a control gate of a regular memory cell,

applying a bias current on a bitline coupled to the regular memory cell,

sensing a voltage on the bitline coupled to the regular memory cell,

applying a third voltage on a common line coupled to the spare memory cell,

applying a fourth voltage on a control gate of the spare memory cell,

applying a bias current on a bitline coupled to the spare memory cell, and

sensing a voltage on the bitline coupled to the spare memory cell.

104. (new) The method of claim 102 further comprising:

checking the value programmed into the regular memory cell against a first set of margin verify values; and

checking the value programmed into the spare memory cell against a second set of margin verify values.

105. (new) The method of claim 102 further comprising:

determining an upper margin verify value corresponding to the received data bits;

comparing a value sensed from the regular memory cell with the upper margin verify value;

indicating the programming success or failure based on a result of the comparing with the upper margin verify value;

comparing a value sensed from the spare memory cell with the upper margin verify value; and

indicating a programming success or failure based on the result of the comparing with the upper margin verify value.

106. The method of claim 102 further comprising:

determining a lower margin verify value corresponding to received data bits;

comparing a value sensed from the regular memory cell with the lower margin verify value;

indicating a program success or failure based on result of the comparing with the lower margin verify value;

comparing the value sensed from the spare memory cell with the lower margin verify value; and

indicating a programming success or failure based on the result of the comparing with the lower margin verify value.

107. (new) A method for programming a multilevel reference memory cell and a multilevel spare cell to a corresponding one of a plurality of levels, the method comprising:

receiving a plurality of data bits;

determining first and second comparison values corresponding to the received data bits;

placing the regular memory cell in a voltage mode;

verifying the regular memory cell using the first comparison value;

if programming is required, programming the regular memory cell with a first programmed value;

if programming is not required, inhibiting the regular memory cell from programming;

placing the spare memory cell in a voltage mode;

verifying the spare memory cell using the second comparison value;

if programming is required, programming the spare memory cell with a second programmed value; and

if programming is not required, inhibiting the spare memory cell from programming.

108. (new) A method for programming a multilevel regular memory cell and an spare memory cell to a corresponding one of a plurality of levels, the method comprising:

receiving a plurality of data bits;

determining first and second comparison values corresponding to the received data bits;

placing the regular and spare memory cells in a current mode;

verifying the regular memory cell using the first comparison value;

after the verifying, if programming is required, programming the regular memory cell with a program value;

verifying the spare memory cell using the second comparison value; and

after the verifying of the spare memory cell, if programming is required, programming the spare memory cell with another program value.